In the claims:

Please cancel claims 5-8.

1. (Original) A printed circuit board comprising:

a plurality of stacked layers; and

a via extending through said stacked layers, said via including a plated through hole located within a predetermined number of said stacked layers and a back-drilled hole located within the remaining stack layers, wherein said plated through hole without an electrically conductive material located on walls therein has a diameter that is substantially the same size or smaller than a diameter of said back-drilled hole.

2. (Original) The printed circuit board of Claim 1, wherein at least one layer of said stacked layers includes a plane layer.

3. (Original) The printed circuit board of Claim 1, wherein at least one layer of said stacked layers includes a signal layer.

4. (Original) The printed circuit board of Claim 1, wherein a plurality of said vias are located within said printed circuit board.

5-8. Cancelled

9. (Original) A printed circuit board comprising:

a plurality of stacked layers; and

a plated hole located within a predetermined number of said stacked layers that was formed by:

drilling a first hole having a first diameter through said stacked layers;

drilling a second hole having a second diameter concentrically around and through a predetermined depth of said first hole;

plating walls of said second hole and walls of a remaining portion of said first hole within said stacked layers; and

back-drilling a third hole having a third diameter concentrically around and through the remaining portion of said plated first hole to remove that portion of said plated first hole and leave said plated second hole which forms the plated through hole.

10. (Original) The printed circuit board of Claim 9, wherein at least one layer of said stacked layers includes a plane layer.

11. (Original) The printed circuit board of Claim 9, wherein at least one layer of said stacked layers includes a signal layer.

12. (Original) The printed circuit board of Claim 9, wherein said second diameter of said second hole is substantially the same size or smaller than said third diameter of said third hole.

13. (Original) The printed circuit board of Claim 9, wherein said step of plating includes applying a layer of conductive material on the walls of said second hole and on the walls of the remaining portion of said first hole and on predetermined areas on a top surface and bottom surface of said stacked layers.

14. (Original) The printed circuit board of Claim 9, wherein a plurality of said plated through holes are formed within said printed circuit board.